VLSI SINCE 1983
2024 International
VLSI
Symposium on
Technology, Systems and Applications
April 22–25, 2024 Hsinchu, Taiwan
ITRI Industrial Technology Research Institute
◆IEEE

DAT Call for Papers

The 2024 International VLSI Symposium on Technology, Systems and Applications will be held on April 22-25, 2024, at the Ambassador Hotel, Hsinchu, Taiwan. Original and unpublished papers on all aspects are solicited, including but not limited to the following scope.

SCOPE

■ Analog, Mixed-Signal, and RF Design
- Analog and Mixed-Signal Circuits
- Power Management Circuits
- Wireless Transmitter and Receiver Circuits
- Wired System and IO Design
- Sensor and Interface Circuits

■ Digital, Memory, and AI Chip Design
- Asynchronous and Neuromorphic Computing Circuits
- Communication Baseband Designs
- Computing-in-Memory
- Digital AI Chips
- Digital Circuits and ASICs
- Hardware Security and Trust
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems
- Security Circuits for IoT and AI
- Specialized Hardware

■ Emerging Technology
- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

■ Application, Software and Hardware, and AI System
- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip)
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration

■ Design Automation and Test Methodology
- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

GENERAL INSTRUCTIONS

- Prospective authors must electronically submit the self-contained paper with figures and tables via the conference submission page (https://expo.itri.org.tw/2024DAT/Submission) before December 6, 2023 (23:59 GMT+8).
- The submitted manuscript must be 2 or 4 pages including references, double-columned, IEEE-style compatible, in PDF format only. Any submissions not adhering to the rules will be rejected immediately without review.
- Before submitting your abstract/paper, please review the information on IEEE Intellectual Property Rights at https://www.ieee.org/publications/rights/index.html
- The review process will be **double-blind**.
  - Please do NOT reveal any authors' information (names, affiliations, email, grant information, personal acknowledgment, etc.) anywhere in the initial manuscript. You must also ensure that the metadata in the PDF does not include such information.
  - All references, including authors' previous work, should be referred as 3rd-persons' works. E.g., you should use "This paper presents a new method to improve XXX's approach [1]." instead of "This paper presents a new method to improve our previous approach [1]." Do NOT omit or anonymize references for blind review.
  - The initial manuscript violating the double-blind review policy will be rejected.
- Accepted papers **MUST** be presented **in person** by one of the authors at the symposium, and the presentation must be conducted in English. All accepted manuscripts in the proceeding will be published in IEEE Xplore.
- Any changes on the title or author list or withdrawal after acceptance must be approved by DAT Program Chairs.
- All paper presenters are required to register for the symposium.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.
- Please refer to the detailed information on the conference website for authors: https://expo.itri.org.tw/2024VLSITSA

STUDENT SUBSIDY

- Student Travel Financial support for attending 2024 VLSI TSA is available for full-time student presenters living outside of Taiwan.

BEST PAPER AWARD

Three best papers will be selected this year through a rigorous evaluation process conducted by the DAT technical program committee and session chairs.

IMPORTANT DATES Note: all are based on Taiwan time (GMT+8).

Paper Submission Deadline	Extended to Dec. 20, 2023
Notification of Acceptance	Jan. 31, 2024
Deadline for Final Paper (IEEE compatible version) Submission	Feb. 28, 2024
Deadline for Author Registration	Feb. 28, 2024

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